REMARKS

Claims 1-22 are pending in the present application.

Claims 2-11 and 13-22 have been allowed.

Claims 1 and 12 have been rejected.

Claims 1 and 12 have been amended.

Claims 1-22 remain in the application. Reconsideration of the claims is respectfully requested. Claims 1-22 are shown in their current form in Appendix A for the Examiner's easy reference.

In Section 1 of the October 31, 2002 Office Action, the Examiner objected to the Abstract of the disclosure because it contain more than 150 words. To correct this, the Applicant has replaced the Abstract with a substitute Abstract containing less than 150 words.

In Section 2 of the October 31, 2002 Office Action, the Examiner objected to Claims 1 and 12 because the claim language "capable of notifying" recited in Claims 1 and 12 is not a positive recitation. The Applicant has amended Claims 1 and 12 to address this issue.

The Applicant hereby requests reconsideration of Claims 1-22 and that Claims 1-22 be passed to issue.

SUMMARY

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***jmockler@davismunck.com***.

Respectfully submitted,

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Date: Jan. 31, 2003

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APPENDIX A

CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A power monitor circuit [capable of notifying] operable to notify processing circuits operating from a first power supply having a VDD output voltage when a second power supply having a VDDIO output voltage is powered up, wherein VDDIO is greater than VDD, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

an odd number of serially connected inverters operating from said first power supply, wherein an input of a first of said serially connected inverters is connected to said voltage divider circuit output node and an output of a last of said serially connected inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.

2. The power monitor circuit as set forth in Claim 1 wherein said serially connected inverters comprise CMOS inverters.

3. The power monitor circuit as set forth in Claim 1 wherein said voltage divider circuit comprises: 1) a first N-channel transistor having a gate and a drain coupled to said VDDIO output voltage and a source coupled to said voltage divider circuit output node; 2) a second N-channel transistor having a gate coupled to said VDD output voltage and a drain coupled to said voltage divider circuit output node; and 3) a third N-channel transistor having a gate coupled to said status signal, a drain coupled to a source of said second N-channel transistor, and a source coupled to ground.

4. The power monitor circuit as set forth in Claim 3 further comprising a capacitor coupled between said voltage divider circuit output node and ground.

5. The power monitor circuit as set forth in Claim 4 further comprising a fourth N-channel transistor having a gate coupled to said VDD output voltage, a drain coupled to said VDDIO output voltage, and a source coupled to said voltage divider circuit output node.

6. The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises one inverter.

7. The power monitor circuit as set forth in Claim 6 wherein said odd number of serially

connected inverters comprises one CMOS inverter.

8. The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises three inverters.

9. The power monitor circuit as set forth in Claim 8 wherein said odd number of serially connected inverters comprises three CMOS inverters.

10. The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises five inverters.

11. The power monitor circuit as set forth in Claim 10 wherein said odd number of serially connected inverters comprises five CMOS inverters.

12. (Amended) An integrated circuit comprising:

core processing circuitry operating from a first power supply having a VDD output voltage;

output stage circuitry operating from a second power supply having a VDDIO output voltage, wherein VDDIO is greater than VDD; and

a power monitor circuit [capable of notifying] <u>operable to notify</u> said core processing circuitry when said second power supply having said VDDIO output voltage is powered up, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

an odd number of serially connected inverters operating from said first power supply, wherein an input of a first of said serially connected inverters is connected to said voltage divider circuit output node and an output of a last of said serially connected inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.

13. The integrated circuit as set forth in Claim 12 wherein said serially connected inverters comprise CMOS inverters.

14. The integrated circuit as set forth in Claim 12 wherein said voltage divider circuit comprises: 1) a first N-channel transistor having a gate and a drain coupled to said VDDIO output voltage and a source coupled to said voltage divider circuit output node; 2) a second N-channel

transistor having a gate coupled to said VDD output voltage and a drain coupled to said voltage divider circuit output node; and 3) a third N-channel transistor having a gate coupled to said status signal, a drain coupled to a source of said second N-channel transistor, and a source coupled to ground.

15. The integrated circuit as set forth in Claim 14 further comprising a capacitor coupled between said voltage divider circuit output node and ground.

16. The integrated circuit as set forth in Claim 15 further comprising a fourth N-channel transistor having a gate coupled to said VDD output voltage, a drain coupled to said VDDIO output voltage, and a source coupled to said voltage divider circuit output node.

17. The integrated circuit as set forth in Claim 12 wherein said odd number of serially connected inverters comprises one inverter.

18. The integrated circuit as set forth in Claim 17 wherein said odd number of serially connected inverters comprises one CMOS inverter.

19. The integrated circuit as set forth in Claim 12 wherein said odd number of serially connected inverters comprises three inverters.

20. The integrated circuit as set forth in Claim 19 wherein said odd number of serially connected inverters comprises three CMOS inverters.

21. The integrated circuit as set forth in Claim 20 wherein said odd number of serially connected inverters comprises five inverters.

22. The integrated circuit as set forth in Claim 21 wherein said odd number of serially connected inverters comprises five CMOS inverters.